



# Verification Roadmapping

**A Report on Industrially-Focussed Project Proposals  
resulting from NMI's Verification Roadmapping Project**

**February 2010**

*An NMI project sponsored by the Electronics KTN*



## **Revision History**

<b>Date</b>	<b>Version</b>	<b>Comments</b>
4 <sup>th</sup> January 2010	0.1	Very early draft version for early review only
7 <sup>th</sup> February 2010	0.9	Draft version for release to all participants for review
26 <sup>th</sup> February 2010	1.0	Final Version

## Summary

This report details thirteen industrially-focussed project proposals. These are the outcome of a series of meetings and telephone interviews held in December 2009 & January 2010 on the theme of Verification Roadmapping.

NMI is now seeking participation from a range of organisations to progress these projects to deliver benefits to the project proposers and the wider verification community in the UK.

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## Acknowledgements

NMI thanks all contributors to this project.

This project was carried out by Dr Mike Bartley from Test and Verification Solutions (TVS) on behalf of the National Microelectronics Institute (NMI) and was kindly sponsored by the Electronics Knowledge Transfer Network (E-KTN).

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# 1 Introduction

## 1.1 Background

The Verification Roadmap project was initiated by the NMI in November 2006. The initial objectives were:

- "looking for experts to provide their thoughts and opinions on a specified topic, encompassing expectations and visions for the future and the challenges/barriers involved in getting there"
- "the outcome will be a coherent set of objectives for Verification in the UK, leading to targeted, applied research projects and closer cooperation with leading edge design groups, EDA suppliers and academia"

The primary focus was on the needs of the UK semiconductor design industry with a medium-term timeframe of 3-5 years.

A pilot meeting was held in Bristol in November 2006 which had good attendance. A further meeting held in Bristol in February 2009 was also well attended. The high attendance at the meetings in Bristol demonstrated the interest in this topic and highlights the fact that verification remains the number one design challenge in hardware development.

In Q4 2009 NMI contracted Test and Verification Solutions (TVS)<sup>1</sup> (using funds provided by the Electronics Knowledge Transfer Network<sup>2</sup>) to undertake the project with the expected outcome being:

- "A report containing targeted, applied research projects leading to closer cooperation with leading edge design groups, EDA suppliers and academia."

The intention is that such a report will encourage collaboration between industry and universities – enabling universities to undertake industrially-relevant research to the benefit the UK semiconductor design community.

A number of round-table meetings attended by verification experts were therefore held in December 2009, backed up by telephone interviews and email questionnaires. From these and earlier meetings, it became obvious that the needs of the community would be best served by focussing on tangible projects rather than an abstract roadmap identifying general trends. The meetings and communications were therefore structured with this in mind resulting in this document which records the outcomes from the roadmapping performed by TVS<sup>3</sup>.

## 1.2 Aim of this document

This document records the projects proposals identified during the Verification Roadmapping meetings held around the UK with the aim of turning these proposals into funded projects to deliver benefits to the project participants and the UK verification community.

## 1.3 Intended audience

The intended audience is both the NMI and the potential project participants. This will allow those potential participants to more clearly identify the projects they wish to participate in.

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<sup>1</sup> "Test and Verification Solutions" (TVS) is a company specialising in Hardware Verification and Software testing. More information can be found at [www.tandvsolns.co.uk](http://www.tandvsolns.co.uk)

<sup>2</sup> The "Electronics Knowledge Transfer Network" (Electronics-KTN) is funded by the Technology Strategy Board to support the electronic design community across the UK (see <http://www.electronics-ktn.com>)

<sup>3</sup> Please note that the project "Title: Coverage directed test generation (Draft written by K.Eder)" was written by Kerstin Eder of the University of Bristol (from an earlier roadmap meeting) and not by TVS.

## 1.4 Structure of this document

The rest of this document contains the following details for each of the potential project proposals:

- **Title:** The title of the proposal.
- **Problem Statement:** A brief summary of the problem that the proposal is addressing.
- **Outline:** An outline of the proposed project.
- **Expected project resources and dependencies** required to undertake the project
- **Expected project outcome/deliverables** from the project
- **Proposer:** The main proposer for the project and the resources they can provide.
- **Potential Participants:** Companies interested in participating and the resources they can provide.

## 2 Title: System level power management top-down

### 2.1 Problem Statement

Power management is currently performed bottom-up by adding design features that can ultimately be used by the software applications. However, there is no way for the software developer to view the effect on power of their architectural/design/coding decisions. This means that:

- It is very hard for software developers to understand the effects of their decisions either in absolute terms (thus making it hard to understand if power budgets have been met) or in relative terms (thus making it hard to trade off different options)
- It is hard for hardware designers to understand the impact of their low power features. Given that these are hard to design and verify such features have a large impact on resource/complexity and time-to-market, it would be useful to understand their ultimate usefulness to the software applications.

Such power views should be made at multiple levels of abstraction through the design flow (TLM, RTL, backend) allowing for early feedback and then increasing levels of accuracy.

### 2.2 Project proposal

#### 2.2.1 Outline

Initially this would require a person to architect and prototype a tool that could take a software application running on a design (probably a SOC), take the data from existing power analysis tools and present the information in a format readily understood by the software engineer.

#### 2.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for one year
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to designs and appropriate tools
- A small amount of management, co-ordination and review resource.

#### 2.2.3 Expected project outcome/deliverables

The expected outcome would be a prototype tool and report.

### 2.3 Proposer

Cadence: Could provide

- The Cadence SOC kit (at various levels of abstraction) together with an RTOS and example applications
- Power analysis tools
- Accelerator

### 2.4 Potential Participants

Mentor Graphics:

- Access to tools/technology together with technical assistance and project management.
- Note that Mentor Graphics believe it would be sensible to combine this project with the project "Title: Performance through the product life-cycle" since the two areas relate to architectural exploration and analysis (System Performance and Power) and so are very closely related.

University of Bristol:

- It looks to me as if there is basic research in this topic. We have a formal model of parts of a processor architecture which could serve as a framework to tack the power consumption info onto. This would allow actual and also relative comparisons at several abstraction levels. The formal framework could also be used as a source for generating higher-level simulation models and tests.
- UofB estimates that this is a 3.5 year basic research project.

### 3 Title: Making AMS simulation practical

#### 3.1 Problem Statement

The simulation times for AMS are far too high and so we use digital models to accelerate the simulation. However, it is hard to establish the accuracy of those models.

#### 3.2 Project proposal

##### 3.2.1 Outline

To investigate different ways of establishing the accuracy of behavioural models of AMS designs. Some examples of how to do this might be:

- Some way of generating the AMS and behavioural models from the same source so that the behavioural model is correct by construction.
- Some form of “formal equivalence” of the AMS design and behavioural model.
- Some limited form of equivalence could be established in a standalone manner which would mean that the behavioural model was “signed off” as accurate for certain aspects of behaviour (e.g. connectivity)

The project would look into the following:

- The differing levels of accuracy required of the behavioural models
- And the different ways of establishing that level of accuracy for different types of designs

Note that an alternative proposal was discussed but not supported by the project proposer and so this proposal has been put into a separate section to find a potential proposer.

##### 3.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for one year
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to designs and appropriate tools
- A small amount of management, co-ordination technical oversight and review resource

##### 3.2.3 Expected project outcome/deliverables

The expected outcome would be a report into the various levels of accuracy required and the advantages/disadvantages of the various methods for establishing that level of accuracy

#### 3.3 Alternative project proposal

Acceleration of the AMS design through parallelisation.

#### 3.4 Proposer

Texas Instruments: Could provide

- Access to AMS and behavioural models that are supposed to match
- Small amount of money
- Tools and licenses

#### 3.5 Potential Participants

Cadence:

- Tool and licenses

Ember:

- Interested in this topic but unable to provide money or tools

University of Bristol:

- This might make an interesting student project as a pilot case study from which a larger project could be motivated. UofB could offer this to our MSc or MEng students next academic year.

## 4 Title: Managing complexity through abstraction

### 4.1 Problem Statement

As design complexity continues to increase it becomes increasingly necessary to move from bug discovery to bug avoidance through the deployment of design at higher levels of abstraction.

### 4.2 Project proposal

#### 4.2.1 Outline

Can we model *industrial strength* designs at higher levels of abstraction and then take them through a demonstrably correct flow to a more established design entry point (such as RTL?).

We would take an existing industrial strength design (such as a CPU or GPU) and model it at a higher level of abstraction and then take it through a design flow and compare it against an existing (RTL?) implementation to discover:

- The ease of verifying the original high level model
- The transformations required in moving from the higher level to the RTL and the ease with which those transformation can be verified
- How well the new design compares to the original in terms of performance and bug rates
- Can you achieve a higher quality design in terms of robustness with satisfactory performance?

#### 4.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for one year
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to existing industrial strength designs to allow for comparison with the newly generated version
- Appropriate tools for higher level modelling, verifying the transformations and comparing the performance of two designs.
- A small amount of management, co-ordination technical oversight and review resource

#### 4.2.3 Expected project outcome/deliverables

A report into:

- The appropriate level of modelling at the higher levels and the effects that modelling decisions have on the final performance of the derived design
- The efficacy with which the higher level models can be verified and that the design transformations can be verified correct

### 4.3 Proposer

ARM:

- Industrial strength designs
- A small amount of money

### 4.4 Potential Participants

Cadence:

- Cadence have already done some research into this topic on smaller designs (such as a DMA)
- They can provide licenses

Elda:

- Elda can contribute part time effort for either engineering or review.

Mentor Graphics:

- Access to tools/technology together with technical assistance and project management.

University of Bristol:

- Note that there are formal methods that are mature enough to support some of these ideas.

UofB has modelled a complete (admittedly small hand-knitted) ISA over several abstraction levels down to code generation for a virtual machine. The refinement was property preserving and UofB used a formal proof tool to establish the consistency between abstraction levels. If this project aims to use a similar approach then Bristol would want to ask the partners for collaboration in putting a grant proposal into the EPSRC.

- This project could be put together with the project on “System level power management top-down”. In fact, back in October and December 2009 we had meetings at Bristol to discuss a grant proposal that covers both these areas. Clearly this proposal is very timely as the same two topics have come up through the Roadmapping initiative. We are currently preparing this proposal in collaboration with Southampton University. We would very much welcome guidance on the proposal and letters of support for this proposal from interested parties. Please contact me at [Kerstin.Eder@bristol.ac.uk](mailto:Kerstin.Eder@bristol.ac.uk) to discuss this further.

## 5 Title: Open source generic verification management tool

### 5.1 Problem Statement

All companies are required to perform some level of verification management for a variety of reasons:

- Verification planning (e.g. mapping of features to test plan to tests/coverage/assertions/properties/etc. to execution results)
- Verification status reporting (plan status, execution status, coverage, bugs, etc)
- Verification signoff (understanding verification status at signoff)
- Verification audit records (provide an audit trail of results)

Verification here could be considered beyond functional verification to other forms of verification: performance; power; timing; etc.

A number of tools exist already on the market but they are tied to particular tool vendor flows and are not sufficiently flexible/configurable to be adaptable to particular user needs.

### 5.2 Project proposal

#### 5.2.1 Outline

To produce an open source, generic verification management tool with underlying database for storage and retrieval of results.

Additions from Bristol:

- The tool could provide data mining facilities beyond verification management to perform accelerated triage. In order to help this activity then additional information such as version control information could be included.

#### 5.2.2 Expected project resources and dependencies

A number of companies have already implemented internal versions of such tools. Their knowledge and experience would be incorporated into the requirements and specification for such a tool. These companies also have existing implementations of such tools. These could potentially form the basis of a new tool.

Expected costs would be:

- Resource to combine existing requirements from various companies into a single requirements specification (approx. 3 months)
- Resource to turn the requirements specification into a design, and the design into a tool re-using existing code where possible.
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- A small amount of management, co-ordination technical oversight and review resource

#### 5.2.3 Expected project outcome/deliverables

Open-source, generic verification tool that meets the requirements of all of the participants.

### 5.3 Proposer

DisplayLink:

- Potentially some student resource.

### 5.4 Potential Participants

ARM:

- Potentially some code from their existing internal tool.

Icera:

- Potentially some code from their existing internal tool.
- Engineering time (as long as it doesn't conflict with business goals).
- Resources at Icera (as long as it doesn't interfere with on-going projects).

Art of Silicon:

- Potentially some code from their existing internal tool.

Ensilica:

- Engineering time for the specification and reviewing phases.

XMOS:

- XMOS have developed their own internal tool in this area which they have been using for some time. They expect to be able to contribute ideas, terminology and their existing verification planning/tracking tools.

University of Bristol:

- We run an MSc in Data Mining and some projects could investigate the collected data to discover cause-effect relationships that might help engineers understand the design/test bench better?

## 6 Title: Design IP verification deliverables

### 6.1 Problem Statement

Design IP, whether internal or external, is now used in most SOC developments. However, from a verification viewpoint it is difficult to assess the quality of the design IP and there are no standard deliverables for helping to verify the integration of the design IP (such as integration tests, machine readable register file description, etc).

### 6.2 Project proposal

#### 6.2.1 Outline

Define a set of deliverables that help the verification team:

- Assess the quality of the delivered design IP
- Help with the verification of the integration of the design IP.

Attempt to make the deliverables into a standard.

#### 6.2.2 Expected project resources and dependencies

Initially it is proposed that a DVClub meeting could be used to generate the set of deliverables. This could be then turned into a proposal.

#### 6.2.3 Expected project outcome/deliverables

A document listing a standard set of deliverables.

The start of the process to standardise that set of deliverables.

### 6.3 Proposer

TVS:

- Use of a DVClub meeting to generate a first pass set of deliverables
- Resource to turn that into a propose standard

### 6.4 Potential Participants

It is envisaged that DVClub attendees would participate in the initial process to define the deliverables. A few selected individuals would then be requested to review a draft proposal.

It should also be noted that the (now defunct) VSIA produced some materials in this area which may be useful (see <http://www.vsi.org> ).

## 7 Title: Low power feature verification

### 7.1 Problem Statement

A wide variety of low power features are being added to designs – such as clock gating; distinct power regions; multi- $V_{DD}$ ; multi- $V_T$ ; frequency and voltage scaling.

This leads to a number of verification challenges – such as ensuring we can go in and out of the various power saving modes; ensuring that isolation cells etc work when a region is shutdown; does state get saved and restored correctly?; is voltage and frequency scaling working during reduced performance requirements?; can we prove equivalence between pre- and post- introduction of the design features.

Although support is being introduced through methodologies such as CPF (Common Power Format) and UPF (Unified Power Format) there are still verification challenges in:

- Being able to apply these latest techniques
- Verifying the latest low power features not yet supported by the methodologies

### 7.2 Project proposal

#### 7.2.1 Outline

To define best practice in power verification for:

- Using the current methodologies (CPF/UPF)
- Verifying new low power features not yet supported by those methodologies

This will then be shared and developed through a shared community portal.

#### 7.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for three months
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to existing industrial strength designs that employ a variety of low power techniques
- Access to the typical tools used during low power verification.
- A small amount of management, co-ordination technical oversight and review resource

#### 7.2.3 Expected project outcome/deliverables

A best practice guide with examples on all aspects of verification of both current and expected future low power design techniques.

Additions from Bristol:

- We could make this into an open community contribution project with freely available resources (course, examples, Q&A,)
- This would require funding for ongoing maintenance of the resource

### 7.3 Proposer

Imagination Technology:

- Access to projects, coverage data and tools/technologies that illustrate these issues for the initial analysis and then for trialling any prototype tools produced
- Potentially grant money for a research person

### 7.4 Potential Participants

Infineon Technologies:

University of Bristol:

- If the designs, examples, etc were available then an interesting student project would be to collect, compare and document these approaches. I would be happy to advertise this to our students next year.

## 8 Title: Performance through the product life-cycle

### 8.1 Problem Statement

The complexity of modern products means it is very difficult to analyse if a proposed architecture and implementation will meet the product performance requirements. For example:

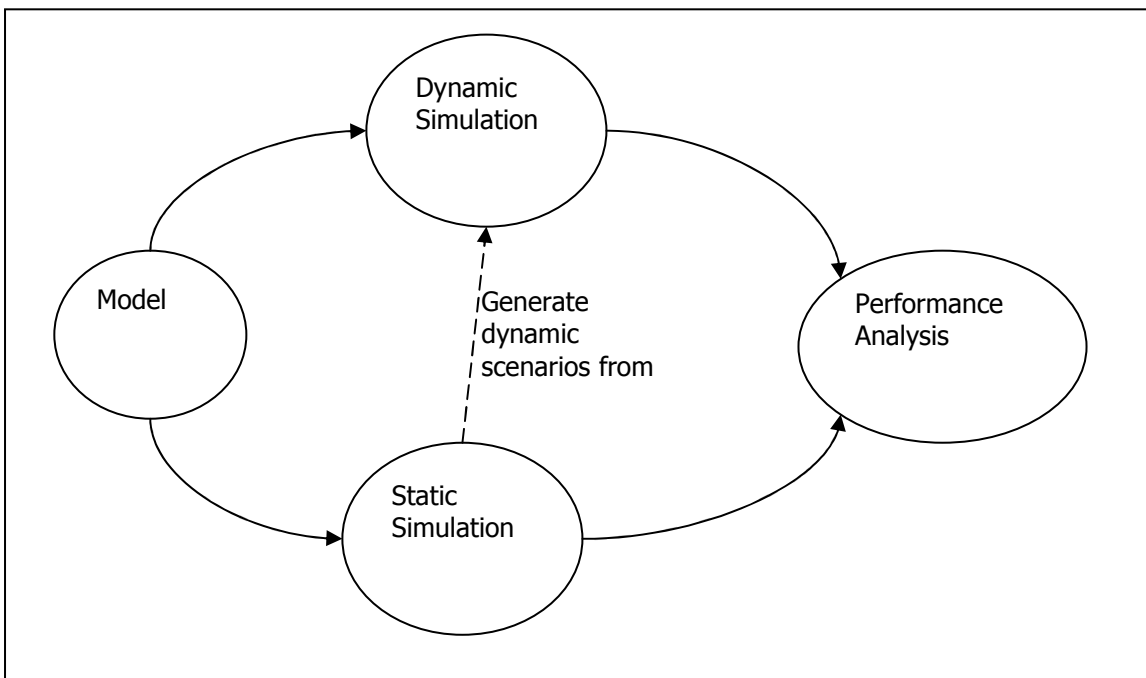
- Are the proposed bus architectures, arbitration schemes and widths adequate?
- Do the proposed memories have sufficient bandwidth?
- What cache settings (size, replacement policy) are sufficient?
- Does a particular function need a HW accelerator or can it be done in SW?

It would be useful to be able to undertake a performance analysis early in the project and carry that through the product lifecycle.

### 8.2 Project proposal

#### 8.2.1 Outline

At a very high level the expected analysis flow is shown below



The initial high-level performance analysis could be performed on a pure bus architecture model with expected data flows annotated. The analysis could then be performed statically or dynamically (with traffic generators and irritators etc.). A worst/best case analysis could then be performed as well as other scenarios.

#### 8.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for six months
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to existing industrial strength projects and project staff for the purposes of understanding requirements and trialling prototypes.
- A small amount of management, co-ordination technical oversight and review resource

### 8.2.3 Expected project outcome/deliverables

A prototype tool for early, high-level performance analysis (static and/or dynamic) with plans for how the tool could be extended to continuous analysis throughout the design flow.

### 8.3 Proposer

Imagination Technology:

- Access to projects, coverage data and tools/technologies that illustrate these issues for the initial analysis and then for trialling any prototype tools produced
- Potentially grant money for a research person

### 8.4 Potential Participants

NXP could provide the following:

- Access to projects, coverage data and tools/technologies that illustrate these issues for the initial analysis and then for trialling any prototype tools produced

Mentor Graphics:

- Note that Mentor Graphics believe it would be sensible to combine this project with the project "Title: System level power management top-down" since the two areas relate to architectural exploration and analysis (System Performance and Power) and so are very closely related.

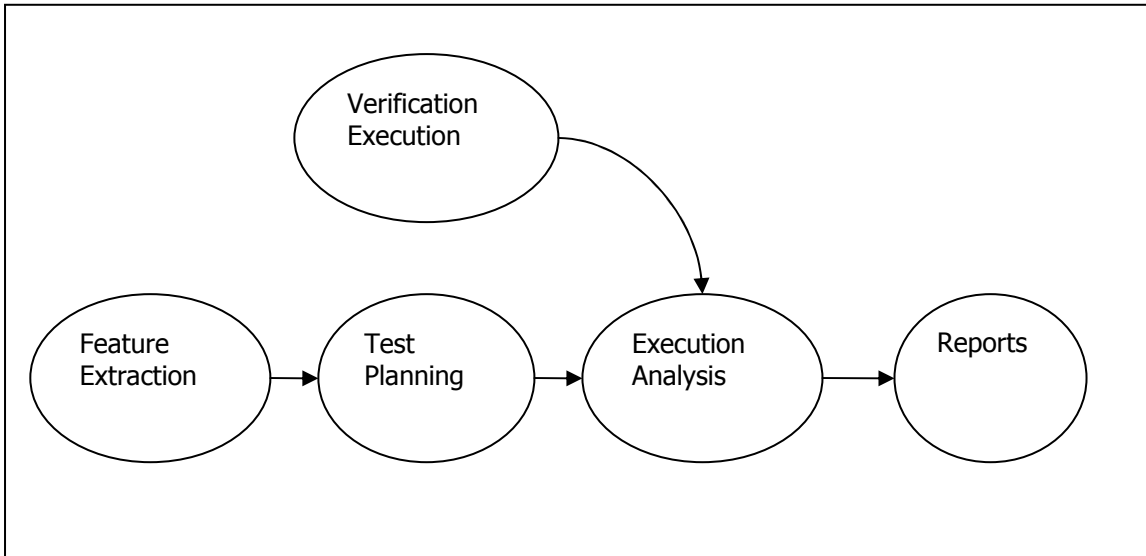
University of Bristol

- This might be a topic for an EngD project (4 year student project with 75% in industry).

## 9 Title: Correlating coverage information from diverse verification platforms

### 9.1 Problem Statement

A number of companies use coverage information to plan their verification, to understand the status both during the project and at signoff, and to redirect resource as/when required.



The problem comes when the verification execution is performed on a diverse range of verification platforms – for example:

- Functional coverage information from simulation
- Execution information from emulation and FPGAs
- Property checking results

The inability to correlate the execution results from these platforms means can lead to inefficiencies (for example through the overlap of verification on the different platforms) and ineffectiveness (for example by not being able to fully analyse where the holes in the verification are).

### 9.2 Project proposal

#### 9.2.1 Outline

The project will first analyse the various types of coverage data produced in verification and propose a means of correlating that information into a single, unified view. It will also propose how that view can be represented in a form that fits in with existing standards for representing coverage data (e.g. the Accellera's Unified Coverage Database Interoperability standard). Finally, the project will produce a prototype tool that facilitates the correlation of coverage into a single, unified view.

#### 9.2.2 Expected project resources and dependencies

Expected costs would be:

- A single research person full time for one year
- Participants to provide input requirements at the start, feedback and guidance during the project, and a final review of the project deliverables
- Access to existing industrial strength projects and project staff for the purposes of understanding requirements, reviewing proposals and trialling prototypes.
- A small amount of management, co-ordination technical oversight and review resource

### 9.2.3 Expected project outcome/deliverables

A detailed technical proposal for how coverage information from diverse verification platforms can be correlated and a prototype tool demonstrating that correlation.

## 9.3 Proposer

NXP could provide the following:

- Access to projects, coverage data and tools/technologies that illustrate these issues for the initial analysis and then for trialling any prototype tools produced

## 9.4 Potential Participants

Imagination Technology could provide the following:

- Access to projects, coverage data and tools/technologies that illustrate these issues for the initial analysis and then for trialling any prototype tools produced
- Potentially grant money for a research person

XMOS:

- XMOS are facing some coverage merging issues between code/functional coverage, different simulators and different test bench environments. XMOS also have to deal with software coverage XMOS are therefore interested in both contributing to and learning from this effort.

TeraStatic:

- Could contribute some help to define goals, and review milestones and final outcome.
- Could potentially also contribute a small amount of money for the research person but cannot commit on that at the moment.

## 10 Title: Professionalising Verification

### 10.1 Problem Statement

Verification is not seen as a distinct profession and career path which leads to a number of issues:

- Verification is not the preferred career option for engineers (design, architecture, etc are preferred)
- There is a lack of verification engineers in the industry
- There is a problem attracting existing engineers into verification
- The skills required by a verification engineer are not well defined which means
  - It is hard to identify similar professions where people could be persuaded to transfer their skills to verification (e.g. software testers)
  - It is hard for engineers to identify how to become a verification engineer
  - Universities are not clear on a suitable syllabus for training engineers to enter into verification once they leave University
- There is no well defined way to assess the ability of a verification engineer

### 10.2 Project proposal

#### 10.2.1 Outline

There will be a number of small projects to professionalise verification with the ultimate aim of increasing the number of engineers entering the profession.

Some examples are:

- A project to define the skills, knowledge and experience expected to be able to perform verification and verification management from entry to varying levels of seniority.  
This could potentially lead to some means of identifying that a person has such skills such as interview guidance or recognized examinations (as happens in other engineering disciplines such as ISTQB for Software Testing)
- A project to define a University syllabus and then provide resources to allow Universities to more easily teach the syllabus.

Other projects could be defined through discussions with the project proposer and participants.

#### 10.2.2 Expected project resources and dependencies

Initially a small amount of effort (approximately one month) would be required to

- define the skills, knowledge and experience required of verification engineers
- define a University syllabus

This could then lead onto a more substantial project to create a University course to allow the syllabus to be taught. The resource required for this would depend on how much existing materials could be re-used.

Additional resource would be required depending on what additional projects are defined and executed after discussion with the project participants.

#### 10.2.3 Expected project outcome/deliverables

- A well-defined set of skills, knowledge and experience required by verification engineers.
- A University syllabus for the teaching of verification.
- Resources to allow for the teaching of that syllabus.
- Other outcomes depend on other what other projects are defined and executed.

### 10.3 Proposer

Art of Silicon

### 10.4 Potential Participants

Mentor Graphics:

TVS:

University of Bristol:

- Note that a DV syllabus already exists at the University of Bristol since 2002. The original syllabus came from IBM/Verisity. The course uses Cadence Specman/e and ncsim in the labs. Students cover a variety of topics. Details can be found online at <http://www.cs.bris.ac.uk/> under Teaching, unit COMSM0115 Design Verification. Participating industrial partners are welcome to evaluate the course materials and to make suggestions. Broadly speaking the unit covers the topics in the book by B. While et al.  
Cadence has selected this course as the leading one for their European Academic Network. As far as I know there are no other universities in the UK or in Europe teaching this material.
- UofB could lead this initiative from the university side and to try to get other universities involved.

## 11 Title: Generic verification scripting environment

### 11.1 Problem Statement

Scripts are difficult to write and maintain, and they can lock us into a particular tool vendor. It would be useful to be able to write scripts at a higher level of abstraction and then allow them to be mapped to particular tools or solutions. This would have the following advantages:

- Scripts could be more easily ported between tools
- Companies could more easily evaluate new tools
- Companies could be more efficient by sharing effort in non-competitive areas

Of course this is not restricted to verification.

### 11.2 Project proposal

#### 11.2.1 Outline

To develop a generic verification scripting API that can then be connected to the various tools used by verification engineers.

The project would first perform a study to identify the typical activities that a verification engineer undertakes. These would then be abstracted into an API.

The next phase would then be to architect a tool that provides an environment for scripting verification tasks and an easy mechanism for implementing the defined API with various tools.

This could be extended to non-verification flows in the future and/or could become part of the "*Open source generic verification management tool*" project.

#### 11.2.2 Expected project resources and dependencies

- *1 month experienced verification engineer.* Initially an experienced verification engineer would be required to identify the typical verification activities into a requirements document and then abstract them into an API.
- *Requirements and reviews by project participants.* All project participants would need to provide verification engineers to take part in the initial requirements analysis phase and then to provide ongoing reviews of the requirements document, the verification API, the tool architecture, tool prototypes and the eventual tool
- *1 year software engineering effort.* This would be initially required to produce a software architecture that can implement the requirements and API, and allow for tools to easily provide the services defined by the API. A prototype would then be developed with the API implemented for a variety of EDA tools. This prototype would then be used for feedback. Finally the feedback and further APIs would be implemented.
- *Project management, ongoing tool management and development.* A small amount of project management would be required during the project. Once an initial tool has been developed and signed off by the various project participants, then there will be an ongoing need to manage the tool development and the environment by which participants share knowledge and code.

#### 11.2.3 Expected project outcome/deliverables

- A generic verification scripting API that can then be connected to the various tools used by verification engineers.
- A tool that provides an environment for scripting verification tasks and an easy mechanism for implementing the defined API with various tools.
- Example implementations of the API for a number of different tools.
- A platform to allow the tool to be shared and to allow people share API implementations.

### 11.3 Proposer

Broadcom could provide the following:

- Engineering time for requirements definitions and reviews

- Money to pay for effort on the project (no money is allocated at this point but potentially could be if Broadcom are part of a consortium that is interested in jointly funding an open source development)

#### **11.4 Potential Participants**

-

## 12 Title: Measuring the effectiveness of constrained random verification

### 12.1 Problem Statement

Pseudo-random verification has become the de-facto state-of-the-art for functional verification and a large amount of time is now spent in the activities required to support this approach:

- Feature extraction
- Defining coverage points
- Writing code to implement those coverage points
- Reviewing, debugging, fixing and maintaining coverage point definitions and implementations
- Capturing and analyzing execution data
- Running extra simulations to try to fill coverage holes or signing off coverage holes

However, it is not clearly understood if this approach is always the most effective or what factors determine the efficacy of this approach.

Another concern is that the functional coverage often requires the use of white box signals and this adds a risk that the semantics of those signals is not clearly understood, adding some risk that the functional coverage semantics are not as expected.

### 12.2 Project proposal

#### 12.2.1 Outline

To undertake research into which factors determine when it is most effective and/or efficient to use a pseudo-random verification approach and when it is better to employ a different approach (e.g. directed, static/formal).

#### 12.2.2 Expected project resources and dependencies

A good approach would be to take industrial strength designs and then apply various verification strategies in order to identify the most efficient. However, this is a very labor intensive approach and it is likely to be more efficient and effective to perform research using the existing experience of verification engineers.

Consequently, the proposal would require 6 month research effort to undertake:

- A literature survey on existing research into
  - where and how various verification strategies are applied
  - comparisons on various verification strategies and techniques
- Interviews with verification engineers into
  - how they decide which technique to apply
  - examples of where the choice had a dramatic positive or negative effect on the efficiency and effectiveness of the verification undertaken
- A means by which to share best practice/tools/techniques.

The project could then look at other ways of directing constraints and/or measuring progress and achieving sign-off such as code coverage, stress sequences, bug coverage and others, all of which seemed to have pros and cons.

#### 12.2.3 Expected project outcome/deliverables

A report on the main decision criteria used to identify when to use a pseudo-random verification approach. An online area where the report can be shared and discussed.

### 12.3 Proposer

Infineon:

- Could give some engineer time, although this would not have to impact project schedules. Access to projects etc should be possible - we already do this for M.Sc. work.
- This may tie in with "Title: Making debug more effective" since information used for debug may be also be useful for coverage (in the same way that assertions and functional coverage look similar).

### 12.4 Potential Participants

University of Bristol:

- If this is put into small enough self-contained projects than these could be offered as MSc projects. We would have to be re-assured that the data plus engineering time for interviews etc are available.

## 13 Title: Making debug more effective

### 13.1 Problem Statement

Verification engineers generally recognize that both they and designers spend a lot of time debugging failing tests and properties. However, there is no real understanding of how much time is actually spent and whether that time is spent efficiently.

### 13.2 Project proposal

#### 13.2.1 Outline

The project would perform a time and motion study initially to understand better how much time verification engineers spend in debug and what types of activity they typically undertake whilst performing that debug. The project would then investigate best practice and tools used for efficient debug, and then look into how to share that best practice.

The project would also consider best practice in ways to avoid bugs being coded in the first place.

#### 13.2.2 Expected project resources and dependencies

- 6 months research resource to
  - Undertake a time-and-motion study across a number of organizations
  - Observe and write-up the best practice/tools/techniques across the industry
- A means by which to share best practice/tools/techniques.
- The project will also require a number of participants to give
  - Time-and-motion information about verification activities.
  - Access to verification engineers to determine best practice
  - Freedom to publish the gathered information (although anonymity will be given)

#### 13.2.3 Expected project outcome/deliverables

A report on typical time spent debugging and the typical activities undertaken during debug.

A report on the best practice/tools/techniques.

An online area where best practice/tools/techniques can be shared.

The project could potentially identify tools that could be used to make debugging more efficient.

### 13.3 Proposer

Infineon

### 13.4 Potential Participants

Note that this project could also be opened up to software testers.

University of Bristol:

- There is a current project that applies machine learning techniques to waveforms in order to spot the difference between passing and failing tests thus automatically leading engineers to the root cause of a test failure. This is only a pilot case study, but if successful could lead to a larger research proposal.
- There might be potential to investigate other approaches towards automating some of the more time consuming aspects of debug. Any suggestions are welcome.

## **14 Title: Coverage directed test generation (Draft written by K.Eder)**

### **14.1 Problem Statement**

Stimulus generation for simulation-based verification is a major bottleneck. The process of coverage closure can consume considerable engineering time and simulation resources. With constraint-based pseudo-random test generation the initial 70% of coverage can often be achieved rapidly. However, gaining the remaining 30% often proves very difficult. Adjusting the bias for test generation requires a high level of skill and design understanding; in practice engineers have to run many trial-and-error experiments to increase coverage. At the end engineers often result to writing directed tests to close the remaining coverage manually. This process is time consuming and can lead to schedule slips. Automatically adjusting the bias for a test generator is a key research challenge.

### **14.2 Project proposal**

#### **14.2.1 Outline**

The project would investigate approaches to close the feedback loop between coverage and test generation. There are already various approaches based on machine learning techniques such as Bayesian networks, Markov chains, evolutionary algorithms and data mining. None of these have made a significant breakthrough. New techniques include approaches based on declarative machine learning and on hybrid methods consisting of probabilistic approaches combined with state machines. These new approaches should be investigated. This is a fundamental research project.

#### **14.2.2 Expected project resources and dependencies**

Full time research project for at least 3.5 years with experienced staff and one PhD student.

#### **14.2.3 Expected project outcome/deliverables**

Understanding of the case-effect relationship between input and coverage for selected DUVs.

Proposal for a method to generalize these relationships.

Prototype tool that implements a method to perform automatic coverage directed test generation based on the above mentioned paradigms.

Evaluation of this method compared to state of the art.

### **14.3 Proposer**

TBD

### **14.4 Potential Participants**

University of Bristol:

- We are currently running a collaborative EngD project with Broadcom in this area. However, we also have some new ideas which can not be covered within the scope of the EngD project. A full research proposal could be submitted to the EPSRC for funding.

## 15 Conclusions

This short project has produced a wide-ranging set of proposals from committed industrial supporters.

From digital and analogue/mixed-signal, touching on software verification, through methodology to design IP, low-power and a project to professionalise verification, these proposals encapsulate the diverse and innovative activities undertaken by the UK semiconductor design community.

NMI now invites interested parties to participate in and support these proposals

## About NMI

The **National Microelectronics Institute** (NMI) is the premier trade association representing the semiconductor industry in the UK and Ireland. Its objective is to help build and support a strong micro and nano-electronics community by acting as a catalyst and facilitator for both commercial and technological development.

A not-for-profit organisation funded by its members, the NMI has a membership that spans the supply chain and includes fabless semiconductor manufacturers, IDMs, foundries, design services, IP providers, business associates, research and academic institutions.

The NMI mission is "To lead the development of a world-class sustainable UK-based microelectronics Systems Design, Device and Manufacturing community providing a compelling value-proposition for our members"

More details are on the website [www.nmi.org.uk](http://www.nmi.org.uk)