DfT Solutions Limited - Profile

DfT Solutions Ltd

DESIGN-FOR-TEST TRAINING AND CONSULTANCY

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Eric Cormack
Managing Director

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DfT Solutions Limited - Training

❑ DfT Solutions Limited:

DfT Solutions Limited provides Design-for-Test(DfT) Training and Consultancy across IC, Board and System test to the Electronics Design communities worldwide.

❑ Training and Seminars:

- Seminars for Managers(1/2 or 1 day duration)
- Training for Design and Test Engineers at Chip and Board Level
- Specialist Courses for Design and Test Engineers
  Boundary Scan at IC, Board and System Level
  Mix-Signal – In development
- Customised Courses and Seminars – Pick the specific test issues you want to learn more about
- Customised Webinar Seminars to maximize your target audience coverage

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DfT Solutions Limited - Consultancy

❑ Consultancy:

DfT Solutions Limited offer a range of test technology and test strategy development consultancy services tailored to solve your Design-For-Test (DFT) and production test challenges.

- DFT reviews and analysis
- Test strategy development
- Design proving
- Production test
- Board Design for Testability
- Board Use of IEEE 1149.1
- Board Test Development
- CJTAG, IJTAG and SJTAG – how their use in today's design environment can improve test and manufacturability

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Overview of the Chip DFT Course

Day 1	Day 2	Day 3
Basics of DFT ❑ DFT, Quality and Test ❑ IC Defects and Fault Models ❑ I_{DDQ} Test	DFT Rule Checking, Delay Faults ❑ DFT Rule Checking ❑ At-Speed Test thru Scan Chains: Path Delay, Transition Delay ❑ ASIC DFT Guidelines	IEEE 1149.1 Boundary Scan Standard ❑ Chip Level Architecture, Board Level Application ❑ 1149.4 Mixed-Signal Test Bus ❑ AMS DFT Review
Internal Scan ❑ Basic Principles ❑ Scan Synthesis Tool Flows	BIST, TDC ❑ BIST Introduction ❑ Memory BIST ❑ Logic BIST ❑ Test Data Compression	Design of Testable SoCs ❑ Test Requirements and Strategies for SoCs ❑ IEEE P1500 Technique: Latest Status ❑ Low-Cost DFT Testers ❑ DFT Life-Cycle View

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Overview of the Board DFT Course

Day 1	Day 2	Day 3
The 1149.1 Boundary Scan Standard Chip-Level Architecture ❑ Motivation ❑ Architecture ❑ BSDL	Other 1149.x-Based Standards ❑1149.4 Mixed-Signal Test Bus ❑1149.6 AC-EXTEST ❑1532 In-System Configuration	Boundary Scan as a Multi-Board Backplane Test Bus ❑ Implementing multi-drop architectures ❑ Case studies
The 1149.1 Boundary Scan Standard Board-Level Application ❑ BS-to-BS ❑ Interconnect Test ❑ BS-to-NBS ❑ Cluster test ❑ Memory test	DFT Guidelines ❑ Chip Level ❑ Board Level ❑ Xilinx-II Pro™	Optional topics ❑1581 SCITT ❑ Board ATE ❑ Live Q&A Sessions

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Overview of the Boundary Scan Course

Day 1	Day 2
The 1149.1 Boundary Scan Standard Chip-Level Architecture ❑ Motivation ❑ Architecture ❑ BSDL	Other 1149.x-Based Standards ❑1149.4 Mixed-Signal Test Bus ❑1149.6 AC-EXTEST ❑1532 In-System Configuration
The 1149.1 Boundary Scan Standard Board-Level Application ❑ BS-to-BS ❑ Interconnect Test ❑ BS-to-NBS ❑ Cluster test ❑ Memory test	Boundary Scan as a Multi-Board Backplane Test Bus ❑ Implementing multi-drop architectures ❑ Case studies

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Proud to be members of the National Microelectronics Institute

Target Audience

Target Audience – Chip DfT Course

- Chip Designers and DFT Engineers
- Chip Test Engineers
- Test-Synthesis Tool Developers
- Project Managers

Assumed Background Knowledge

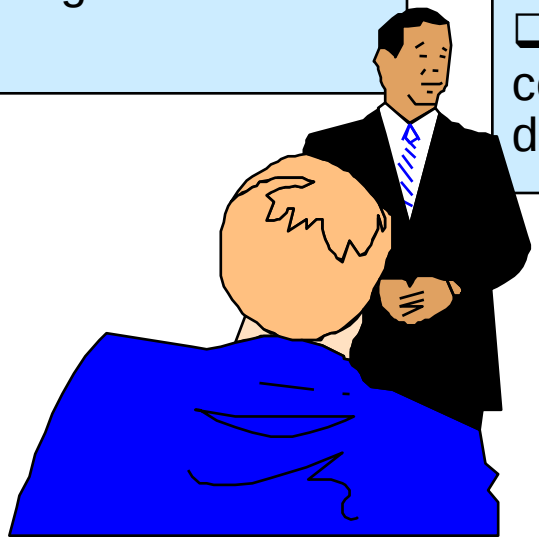
- Principles of logic design and synthesis tool flow

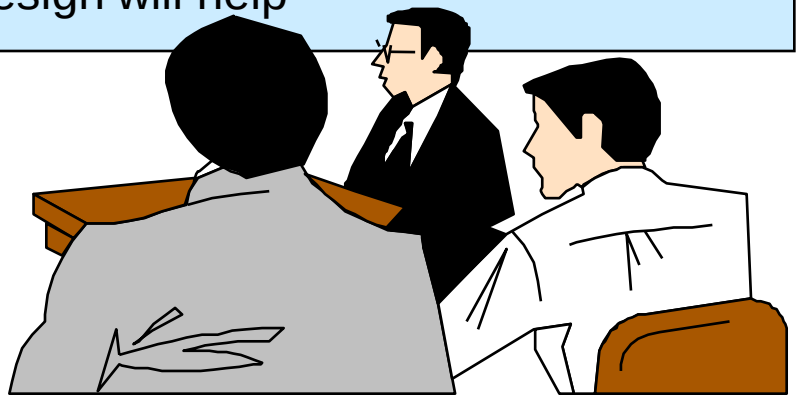
Target Audience – Board DfT Course

- Chip and Board Designers
- Board Test Engineers
- Product Engineers
- Project Managers

Assumed Background Knowledge

- Chip/board design principles
- Some experience with in-system configuration and/or mixed-signal design will help





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About The Author: Eric Cormack

Eric Cormack is an independent consultant in Design-for-Test (DfT), Design-for-Manufacture (DfM) and Design-for-Debug (DfD) consulting in product life-cycle DfT strategies, and delivering on-site and open educational courses in DfT technologies.

Previously, he has worked for Ferranti Computer Systems, Testech, General Hybrid, GenRad, Hitachi Micro Systems Europe, and Philips/NXP Semiconductors. Between 1981 and 1986, he was a test solutions consultant for Testech in the USA establishing offices on East and West coasts. During this time, he was responsible for providing DfT training and consultancy for both commercial and military companies. He then came back to the UK and worked with GenRad as a tools developer and trainer, established a DfT group in Hitachi Micro Systems Europe and provided DfT, DfM and DfD solutions to complex SoC DVB devices for TV/Video applications within Philips/NXP Semiconductors.

He is a core-group member of **SJTAG.**

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