



Verification Technical Network
Low-Power Verification
 Thursday 26th February 2009
 STMicroelectronics, 1000 Aztec West, Bristol, BS32 4SQ

NMI network events provide opportunities for professionals to meet, exchange views and debate the issues.

Event Theme

Design-for-(low)-power is now a common part of the design process. Indeed, NMI has run two events on this subject in recent years. But what about verification of a low-power design? What impact do design techniques for low-power have on the verification process? And how can you verify a system with multiple voltage domains, any of which can be powered-down independently?

This event will look at the challenges and pitfalls facing those who not only have to verify the 'normal' functional behaviour of a system but also handle the complexity introduced by low-power designs.

As with all NMI Technical Network events, there will be opportunities to meet and network with attendees from a variety of organisations.

Agenda

<p>09:00 Registration <i>Refreshments, Networking & Sponsor Table-Tops</i></p> <p>9:45 <i>Welcome & Introduction</i> Robin Kennedy, NMI</p> <p><i>Introduction to Low-Power</i> Chris Clarke, University of Bath</p> <p><i>An Overview of the Verification Challenges Posed by Low-Power Design</i> Mike Bartley, TVS</p> <p>10:50 Break</p> <p>11:15 <i>Metric Driven Low Power Verification</i> Michael O'Sullivan, Cadence Design Systems</p> <p><i>GPS 24/7 and Low-Power Verification – the Air Way...</i> David Tester, Air Semiconductor</p> <p><i>A Low-Power Verification Flow Using UPF</i> Nigel Elliot, Mentor Graphics</p>	<p>12:40 Buffet Lunch & Networking</p> <p>13:40 <i>The Implementation of Power Aware Verification on Digital SoC</i> Pondori Kurade, ST-Ericsson</p> <p><i>Low Power Design may be challenging but Low Power Verification doesn't have to be</i> Bhavesh Patel, Synopsys</p> <p>14:30 Break</p> <p>15:00 <i>Evaluation of low power verification techniques on a microcontroller-based SoC</i> Alan Whooley, Analog Devices</p> <p><i>Verification in a Clock Gating Based Low Power Flow</i> Richard Langridge, Calypto Design Systems</p> <p>16:00 Prize Draw & Close <i>Continued Networking</i></p>
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Event Sponsors:



Event Supported by STMicroelectronics & Zuken

For further details, please contact Robin Kennedy
Tel: +44 (0)789 48 99 5 44 email : robin.kennedy@nmi.org.uk