



Analogue/Mixed-Signal/RF Technical Network

Leading Mixed-Signal Designs down the Sub-Micron Path

Thursday 2nd April 2009

Intel, Pipers Way, Swindon, SN3 1RJ

NMI network events provide opportunities for professionals to meet, exchange views and debate the issues.

Event Theme

Analogue and Mixed-Signal Designs are often best implemented in mature, well established technologies. Indeed, moving such designs to smaller geometries can be difficult and lead to an increase in the size of analogue blocks as more circuitry is required to achieve previous performance. However, there is often little choice as the drive for economic benefits through increased integration and enhanced functionality in the digital section means that the analogue portion simply has to keep in step with the digital.

This event will look at the challenges, issues and opportunities in both porting existing and creating new designs in deeper sub-micron technologies, including modelling and co-simulation. Along the way, we will be questioning whether it is always appropriate that analogue designs should track the digital.

As with all NMI Technical Network events, there will be ample opportunities to meet and network with attendees from a wide variety of organisations.

Agenda

09:00 Registration

Refreshments, Networking & Sponsor Table-Tops

9:45

Welcome & Introduction

Robin Kennedy, NMI

Analogue at the Bleeding Edge,

Paul Double (session chair)

The economic limitations of deep sub-micron integration for Analog and Mixed signal technology

Simon Atkinson, Mirics Semiconductor

60 GHz: Applications and Sub-Micron IC technology

Mark Barrett, TES Electronic Solutions

Flexible Technology for Mixed-Signal SoC Verification

Barry Byford, Mentor Graphics

Mixed-Signal SoC Verification - modelling & methodologies

Steve Crosher, Moortec

Addressing the Shortage of Analogue Skills

iSLI, Diarmuid O'Connell

12:00 Buffet Lunch & Networking

Introduction to RF/MS design at Intel UK

Richard Goldman, Intel

Constraint-based Analog IC Design

Ian Clifford, Cadence

Yield and DFM in Layout at Nanometer Technologies

Adrian O'Shaughnessy, IC Mask Design

Producing robust, high yielding, analog IC designs in sub-micron processes

Jeremy Sonander, Saros

14:15 Break

Interoperable PDK Libraries - OpenAccess for deep sub-micron

Damian Roberts, Synopsys

Panel Session (chaired by Peter Saul, SaulResearch)

"Mixed-Signal in Deep Sub-Micron – Why? How?"

16:00 Prize Draw & Close

Continued Networking

For further details, please contact Robin Kennedy

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