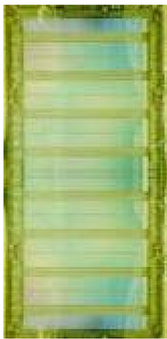
National
Microelectronics
Institute

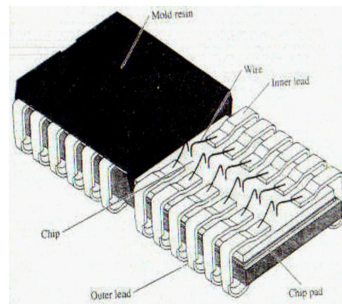
TWI

25th May, Cambridge

“Lifting the Lid on Product Design”
IC Package & System Level Design Network

Delegate Handbook





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1 Introduction & Welcome to NMI "Lifting the Lid on Product Design 2010"

NMI is delighted to introduce a combined IC Package / System-Level Chip Design Network event on the theme "Lifting the Lid on Product Design". This will be a unique opportunity to learn about the challenges and enabling solutions being implemented from Chip to Package to Product in today's highly complex technologies.

In addition to our line up of exciting talks we invite you to get your questions ready for an exciting Panel Debate on the topic "The Perfect Product …. ?"

Don't miss this opportunity to learn about the future of Product Design and how Engineering teams are evolving to meet the needs of the Consumer.

We hope you enjoy the event and we welcome your feedback to ensure we deliver the Network activities that are your priority !

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National Microelectronics Institute
Building and Uniting a Strong Microelectronics Community

www.nmi.org.uk

2 Agenda

Network Event Co-Hosted TWI

"Lifting the Lid on Product Design"

System-Level Chip Design & IC Package Network

Book the Date: Tue 25th May 2010

Location: TWI (McClintock Building), Great Abington, Cambridge, CB21 6AL

Event Theme

Agenda

Time	Session	Speaker
9:00	**Registration & Coffee – Networking and Sponsor Tabletops**	
9:30	Introduction and Welcome address	Robin Kennedy/Paul Jarvie, **NMI**
	Everything Including the Chip	Jonathan Edwards, **ST-Ericsson**
	One Foot on Sea, and One on Shore	Paul Freeman, **Icera Semiconductor**
	Reducing Development Schedule by Rapid Prototyping	TBC, **Synopsys**
11:05	**Break**	
	Sounds Good? Audio solutions to connect the real world to the digital world.	Eddie Sinnott**, Wolfson Microelectronics**
	Improving Workflow in Embedded CE Audio Processing	John Richards**, Oxford Digital**
12:30	**Lunch**	
	From Concept to Production	Azmi Mohd Isa & Brian Morris, **Unisem**
	Using Standards & Designing for Compliance	Alan Powell**, Wemtech**
	System Design has Evolved	Adrian Harper, **Mentor Graphics**
14:50	**Break**	
	Strategy for Integrated Passives	Andy Whittaker, **TWI**
	New approaches to solving chip-package-co-design challenges	Janez Jaklic, **Cadence**
	Panel and Q&A Session: "The Perfect Product… ?"	
16:30	**Close & Further Networking**	

For further details, please contact Sophie Ericson at : **sophie.ericson@nmi.org.uk** +44 1506 401214

Event Sponsors & Supporters:

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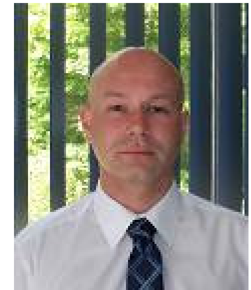
3 Speaker Biographies

Adrian Harper, *Mentor Graphics*

Adrian Harper is a European Application Engineer for Mentor Graphics. He represents the PCB hardware development process for the Systems Design Division in a Business Development role. He works with leading global electronics companies in Europe and India at a technical management level helping customers address their development needs for low, medium and high volume products.

Alan Powell, *Wemtech*



Alan studied at the University of Birmingham before working with a small process & production efficiency firm based in Telford. Following a spell at De La Rue Cash Systems he spent nearly 5 years with British Standards Product Services, mainly in the Engineering department dealing with enquiries from around the globe. Alan has been with Wemtech since 1st September 2008. If you recognise Alan, you may have seen him at their regular seminar slots at the regional manufacturing shows organised by ETES.

Andy Whitaker, *TWI*

Andy Whitaker is Consultant and Technology Manager (Micro technology) at TWI Ltd, where he has special responsibility for electrical and electronic products, their manufacture and reliability. Prior to joining TWI he was Engineering and Commercial Manager for Smiths Aerospace Microcircuits (Newmarket).

Azmi Mohd Isa, *Unisem*

Azmi graduated in 1991 with BBA (Hons) with Prof.Dip Marketing (CIM). He has more than 21 years experience in sales and marketing for semiconductor sub-contract assembly and test."

Brian Morris, *Unisem*

Brian is currently employed as Technical Program Manager for Europe at UNISEM, based in South Wales. He graduated with Master of Engineering from the University of Glamorgan in 1995 and started in the New Model Introduction department of SONY Electronics, Pencoed. He then moved to LG Electronics and worked on assembly process development for the Apple iMac. Brian started with UNISEM as a wire-bond process engineer, and then moved department to become responsible for technical support for fabless and large IDM customers. He has almost 10 years experience of semiconductor assembly.

Doug Amos, *Synopsys*

Doug joined Synopsys as part of the Synplicity Acquisition in 2008. Previously at Synplicity, Doug was the first engineer and Technical Director in Europe, responsible for all ASIC and FPGA Field Application Engineering support. For 5 years prior to joining Synplicity, Doug managed the European FAE force for Altera having previously held various consulting and engineering positions focussed on FPGA and working with Actel, Altera, and Xilinx.

Doug has an honours degree in Electrical and Electronic Engineering from the University of Bath, England and is a proud 25-year veteran of FPGA and ASIC design

Eddie Sinnott, *Wolfson Microelectronics*

Eddie has 17 years experience in the global semiconductor market, having held a variety of senior business development, product marketing and product management positions across Europe and the US. Eddie spent 15 years with Freescale Semiconductor (formerly Motorola Semiconductor) in the hugely competitive $10Bn Microcontroller market, developing and marketing products for Automotive, Industrial and Consumer customers. In 2008 Eddie became a Homecoming Scot, returning from 4 years in Austin, Texas to take up the Director of Product Management role with Wolfson Microelectronics in Edinburgh, Scotland's largest indigenous Semiconductor company providing high performance mixed-signal semiconductors to many of the world's most recognized consumer brands.

With a degree in Laser Physics and Optoelectronics from Strathclyde University and an MBa from London Business School, Eddie has extensive experience in developing market, customer and product requirements for complex technology products in fast moving segments then bringing these products successfully to a global market.

Janez Jaklic, *Cadence*

Janez Jaklic is a senior services manager leading the European SPB services team at Cadence Design Systems, GmbH. For over 5 years his focus is on methodologies for SiP design, chip-package-board co-design and DFM for IC packaging. Prior to that he was working for 7 years in different areas of custom IC design, parasitic extraction, physical verification and custom software development. He received his BSc and PhD in physics from University of Ljubljana.

John Richards, *Oxford Digital*

John graduated with an Honours Degree in Electronic Engineering from Leeds University followed by an MTech in Digital Signal Processing from Brunel University.

Having spent 10 years at EMI's Central Research Labs leading a variety of cutting edge projects including the world's first ALL-digital Audio Mixing Desk, John changed career completely and joined Sony's Advanced Development Group in Basingstoke pioneering digital video technology including High Definition Non-Linear Special Effects and High Definition Motion-Compensated Standards conversion.

From being head of the Video R&D Department in 1990, John returned to audio in 1993 with a new challenge as head of the newly formed Sony Pro-Audio R&D Lab, Oxford. The main mission was to develop and productise the OXF-R3 Mixing Console; this was launched as a commercial product within 2 years.

The work of the group was diversified into many other areas and in 2001 the Lab became a commercial unit running businesses on a worldwide basis including a software retail business in workstation plug-in software and licensing activities with 3rd Party Partners alongside development of Core Technology for many of Sony's international companies in both professional and consumer areas.

John left Sony at the end of June 2006, together with a colleague, Peter Eastty, having effected a spin out of the part of Sony's Pro-Audio Lab concerned with Pro-Audio R&D and audio effects for consumer A/V to form Oxford Digital Limited, a company specialising in audio technology licensing and contract engineering for strategic partners.

Some clients that are public include: D&M Holdings Inc., Dialog Semiconductor, Sony Corporation, Sony Ericsson Japan, SRS Labs Inc., Texas Instruments Inc. and Yamaha Corporation.

John is a Fellow of the IET, a Chartered Engineer, a Senior Member of the IEEE and a Fellow of the Royal Television Society.

Dr Jonathan Edwards, *ST-Ericsson*

Dr Jonathan Edwards is Physical IP Manager in the CTO and Strategic Planning Office of ST-Ericsson. He is currently based in Bristol and Grenoble. During his career in microelectronics spanning over 33 years with Plessey, Inmos, ST and now ST-Ericsson he has been involved with CCD, NMOS and CMOS technologies ranging from 7 m down to 28nm, specializing on process and device definition and modelling, logic and memory design, and managing graphics, microprocessor, memory and EDA design teams in the UK, France and Italy.

Paul Freeman, *Icera Semiconductor*

Paul Freeman has worked in the semiconductor industry since joining inmos/ STMicroelectronics in 1988. He joined Element 14 in 2000 with responsibility for packaging, test and product engineering. A few years after acquisition by Broadcom, he joined several ex-Element 14 engineers at Icera in 2004 with the same set of responsibilities. Icera is now shipping high volumes of the world's highest performing 3G wireless modem chipset to the world's leading cellular terminal suppliers.

4 Presentation Abstracts

Adrian Harper, *Mentor Graphics*

'System Design has evolved'

Picture your typical electronic design engineer with a desk stacked with electronic data books, specifications, schematic drawings, prototype test boards & test equipment…remember that?

System Design had to evolve significantly to survive today's aggressive, cost conscious, fast edge rate and multi-functional driven market. First on the shelf is everything, second is nothing.

To bring product to the market more quickly than ever before it is no longer tenable to design in a serial hand-over process. Producing prototypes take weeks to test, modify, re-spin and iterate the process to result in a board that either works to specification or has the specification changed to match the results of the board. System Design has evolved to support multi-discipline collaboration, working in parallel with engineering experts, suppliers and third party developers both locally or globally. System design now supports virtual prototyping through simulation, analysis and modeling the performance of system long before any physical implementation is produced. And today the route to manufacturing is equally seamless.

This presentation lifts the lid on design processes for PCB which are at the heart of all complex electronic products. It explores today's design challenges which you must face to evolve or face the prospect of extinction.

Andy Whitaker, *TWI*

'Strategy for Integrated Passives'

Integration of passive devices into electronic substrates is gaining widespread adoption for high-density products. This contribution reviews two approaches to a cost effective implementation for PCB and Silicon Substrates as explored in the ADEPT-SiP and PPM2 projects supported by TSB. New test methods are required to support product design and qualification using IP technologies, with special emphasis on reducing time to market.

Azmi Mohd Isa & Brian Morris, *Unisem*

'From Concept to Production'

Product development companies have a strong focus on marketing and development, whilst often leaving the choice of packaging for their product until the end of the design cycle. The choice of packaging can be crucial, and many factors need to be considered from the start.

These include physical die layout, thermal and electrical requirements, device testing, cost and end user requirements. Involving the chosen assembly partner from the start of a new project will result in a product design and package choice that will meet all these criteria, and market expectation. “From Concept to Production” will discuss these factors in detail, and enable good packaging choices to be made.

Doug Amos, *Synopsys*

‘Reducing Development Schedule Using Rapid Prototyping’

This NMI Network event is intended to consider matters beyond purely chip design and as our contribution to the discussion, we would like to highlight the use of FPGAs to create a pre-silicon rapid prototype of a chip design. Whilst offering some general overview of the benefits of rapid prototyping, we will spend most of the presentation relating the recent experience of a real prototyping project at DisplayLink..

In this design case study, we see how rapid prototyping is on track to slice 6 months off the development schedule and to bring early access to software engineers, partners, investors and potential end-customers for a leading-edge DisplayLink product.

Eddie Sinnott, *Wolfson Microelectronics*

‘Sounds Good? Audio solutions to connect the real world to the digital world’

In 2010 almost 3 billion consumer electronics devices – in your home, in your car, on your person – will be sold. Whether it’s playing music, games, recording or playing back your home movies, playing your favourite ringtone or telling you which way to turn at the next junction: almost without exception, these devices will either “speak or be spoken to” and as such need mixed-signal semiconductor content to manage the audio path. Whether it’s maintaining the quality of the sound as it travels between the real world and the digital world or ensuring the seamless control of the myriad of combinations of audio signals and outputs, the semiconductor responsible for delivering that sound to and from the user must be a deeply integrated part of the overall system.

As the world’s leading provider of mixed signal semiconductors to some of the largest consumer brands in the world, Wolfson Microelectronics works closely with customers during their system level design to ensure the optimum combination of performance, power, size and cost is delivered at a board level. During this session we will explore some of the challenges of delivering a true solution, not just a “chip”.

Janez Jaklic, *Cadence*

'New approaches to solving chip-package-co-design challenges driven by collaboration with industry and academia'

Integration of multiple IC, discrete components and embedded passives in a single package poses significant challenges not only with respect to technology, but also with design tools and methodology. Design as well as feasibility and final verification analysis of the system interconnect in terms of routability, signal integrity and power integrity require a methodology to co-design and analyze the IC and the package in close connection. The ability to implement passives in the package substrate calls for an approach to generate device layouts with required properties automatically and simulate them as part of the whole system. The definition of a SiP design and verification platform has to be extended by combining signal and power integrity analysis for ICs & IC packages into a common environment. Finally, in the view of the complexity of such tightly integrated systems, the verification of the various physical constraints only remains manageable by formalizing them in a dedicated design rule language. We will present how these challenges have been addressed with the partners from industry and academia in two collaboration projects, MOCHA and DIONYSYS.

John Richards, *Oxford Digital*

'Improving Workflow in Embedded CE Audio Processing'

The presentation takes the improvement of sonic performance of consumer AV devices as a case study. Options for implementing DSP algorithms and using pre-configured tuning tools are discussed with respect to minimising time-to-market.

Jonathan Edwards, *ST-Ericsson*

'Everything Including the Chip'

The level of performance, coupled with the wide range of functionality and miniaturization required by today's mobile wireless devices requires a level of integration that cannot be achieved by Moore's law scaling alone. 3D SOC and advanced packaging solutions are needed to increase the effective device packing density. In this talk we briefly review the die stacking solutions in production today, and then look at how the development of the TSV (Through Silicon Via) and fine-pitch bumping technologies are driving a new level of 3D IC integration which can enable repartitioning of the system to meet ever increasing performance and packing density needs. For ultimate device miniaturization, we then present the embedded wafer level ball (eWLB) grid array technology developed jointly by ST, Infinion and STATSChipPAC. These 3D IC and advanced packaging solutions present many new challenges associated with thermal dissipation, thermo-mechanical matching and power and signal distribution, and require the development of sophisticated 3D simulators and co-design tools which can model heterogeneous technologies in a single EDA framework.

Paul Freeman, *Icera Semiconductor*

'One Foot on Sea, and One on Shore'

A semiconductor product's package bridges the gap between the IC and the other components of the system that it is part of. It is becoming an increasingly significant part of the unit cost of the semiconductor product. This in turn might also be a significant part of the cost of the finished product that it is part of. However, the level of investment required in specifying and developing a semiconductor product's optimal package is often underestimated or ignored by companies preoccupied with concept, function and survival. Icera has paid close attention to packaging issues throughout its history and has developed close relationships with its package suppliers. This presentation describes key lessons that have been learnt through this time and some of the principles and practices that are applied to Icera's packaging strategy.

5 Exhibitors

Cadence Design Systems

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D-85622 Feldkirchen
Germany

Cadence enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence Allegro technology, methodologies, and services to design many of today's latest electronic products, from advanced SiP's to ultra-dense PCBs.

Synopsys

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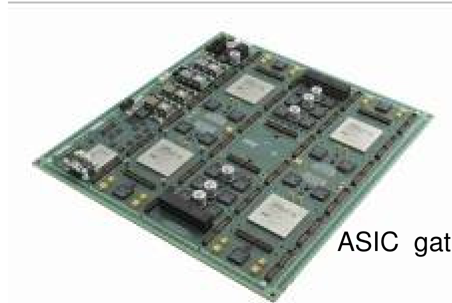
Reading
Berks RG2 6UJ

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing.

Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results.

At this NMI event, Synopsys is particularly focused on their Confirma platform for enabling the early prototyping of SoC, ASIC and FPGA-based system designs. On display are hardware and software components of the Confirma Platform and technical and commercial staff are on hand to answer your questions.



18million ASIC gate Confirma board

These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk.

Synopsys is headquartered in Mountain View, California and the UK offices active in Research, Development, Sales, Support and Consulting are in Reading, Hatfield and Livingstone.

Ansoft

Contact: Charles Blackwood

Email: charles.blackwood@ansys.com

Web: www.ansoft.co.uk/signal_integrity_design.cfm

Tel: 01344 767 550

Ansoft is a leading developer of high-performance electronic design automation (EDA) software, used to design state-of-the-art electronic products, such as cellular phones, Internet-access devices, broadband networking components and systems, integrated circuits (ICs), printed circuit boards (PCBs), automotive electronic systems and power electronics.

Ansoft technology can handle the complexity of modern interconnect design from die-to-die across ICs, packages, connectors and boards. By leveraging advanced electromagnetic-field simulators dynamically linked to powerful circuit and system simulation, engineers can understand the performance of high-speed electronic products long before building a prototype in hardware. This approach enables electronics companies to achieve a competitive advantage with faster time to market, reduced costs, and improved system performance.

The risk of design re-spins can be substantially reduced using the industry-standard electromagnetic software Ansoft HFSS™ (www.hfss.co.uk). HFSS is widely used for analysing full 3D field behaviour of electronics modules including packages, interconnects and PCBs, and extracting S-parameter and full-wave SPICE models .

For very complicated full board and package structures Ansoft SIwave (www.siwave.co.uk) allows similar extraction capabilities. The coupling of SIwave and HFSS allows full signal and power integrity analysis of a complete complex package / PCB and its housing.

Ansoft tools can improve engineering productivity, reduce development time and better assure first-pass design success.

Eltek Semiconductors Ltd

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Web: www.eltek-semi.com

Tel: +44 (0)1803 837072

Address: Nelson Road Industrial Estate
Dartmouth
Devon
TQ6 9LA

Services Offered: Test program development. Wafer probe test. Wafer sawing & offload. Device assembly into ceramic, metal & plastic packaging. Final electrical test. Screening. Burn-in. Life test. Long established & fully equipped UK facilty.

Scale: Prototypes to volume production in a variety of package styles. Transition to high volume can be supported via partners in Europe & Far East.

Market areas: From commercial to specialised. Experience in hi-reliability Defence, Space, High temp applications. MEMS assembly capability.

Value Added Services: Eltek also provides fab-less semiconductor customers with services such as die storage, inventory management and distribution.

IMAPS-UK

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SP10 5NY

The International Microelectronics And Packaging Society (IMAPS) is the largest organisation dedicated to the advancement and growth of microelectronics and electronics packaging. The United Kingdom Chapter (IMAPS-UK) provides a forum for its members via seminars, conferences, newsletters, website's etc., to ensure they are kept up to date with the latest news, developments & innovations in our field.

Oxford Digital Limited

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Web: http:// www.oxford-digital.com

Tel: 0845-450-5664

Address: 1, Farley Lane
The Ridings
Stonesfield
Oxfordshire
OX29 8NP

Oxford Digital is a technology company that specialises in digital audio signal processing for consumer electronic products. We offer semiconductor manufacturers both consultancy services and licensing of audio DSP which includes: an extremely compact audio DSP core, a rapid programming and development environment (or direct implementation in silicon from MatLab Simulink), audio effects and back-end Tuning Tools that allow rapid optimisation of the sonic performance of CE equipment.

Technologies Served

All types of embedded digital audio signal processing

PHASIX

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GU34 5AZ

Driven to serve our customers' need for rapid, accurate and comprehensive test results Phasix is a growing semiconductor test and analysis outsource partner.

Located across two centres in Hampshire and Devon, Southern England, our experienced team is waiting to provide you with ESD and FA services for device characterisation, qualification and control.

Phasix ESD focuses on Semiconductor Quality and Reliability, helping our customers ensure their products are sufficiently robust to guarantee reliability in their intended end-use and offers….

- A full suite of ISO accredited testing services which includes HBM, MM, CDM and Latch Up with optional I-V Curve Tracing
- A highly responsive and flexible service with 5 days-or-less guaranteed turn time, from receipt of samples to delivery of results
- The maximum useable information about the ESD sensitivity of your devices
- On site service, repair and calibration of your in-house ESD test equipment
- Sound advice on the selection of appropriate testing standards and methodologies when you need it

Phasix FA focuses on the provision of rapid Failure Analysis services for the diagnosis of ESD failures, customer returns, potential competitor patent infringements, counterfeit detection and circuit edit for 'first silicon' design modifications. The range of capabilities, often delivered within 48 hours includes….

- Non-destructive package inspection using real-time X-ray and Optical Inspection
- Non-destructive package analysis using Surface Acoustic Microscopy (CSAM)
- Device decap using acid or jet etch to dissolve the mold compound
- Layer-by-layer device deprocessing using plasma etch, wet etch and mechanical polishing
- Imaging using a range of microscopes including Scanning Electron Microscope (SEM)
- Materials elemental analysis using Energy Dispersive X-Ray (EDX) capability
- Failure location using photon emission microscopes and liquid crystal thermography
- Circuit editing for silicon debug and repair using Focused Ion Beam (FIB)
- Structural and defect analysis by cross sectioning using the FIB
- Voltage Contrast analysis using FIB for checking continuity of interconnect layers
- Fine surface analysis using Atomic Force Microscopy (AFM)
- Cross sectioning including TEM sample preparation using the FIB
- Transmission Electron Microscope (TEM) imaging of thin silicon slices down to 0.4nm resolution

RoodMicrotec

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Web: www.roodmicrotec.com

Tel: 07785 341322

Address: RoodMicrotec Stuttgart GmbH.
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70499 Stuttgart
Germany

RoodMicrotec GmbH offers Test programme development, engineering, qualification, failure analysis and FIB to the Fabless community. Based in southern Germany the company offers dual site security and UK representative support.

TWI

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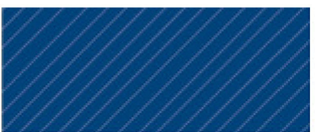
CB21 6AL

TWI is an internationally recognised research and development company that supports over 3500 organisations in 80 countries. It specialises in materials, joining, assembly, training and technology transfer. With 40 years experience in electronics, sensors and medical devices it provides services in many packaging technologies including:

Electronic and sensor interconnect and packaging
High temperature harsh environment systems
Thermal management
Integrated passives
Precision reliability testing
Product prototyping
Troubleshooting & Failure analysis

6 UKESF: The UK Electronics Skills Foundation

UKESF: The UK Electronics Skills Foundation



A collaboration between industry, academia and the public sector:

- Working towards a sustainable supply of quality, industry-prepared graduates
- Attracting young people to degree study and professional careers in electronics
- Connecting employers with young talent in schools and universities

Why was UKESF set up?

To address the threat of diminishing skills capability in the UK electronics sector

UKESF is addressing the risk posed by the recent and sharp decline in the numbers of UK students accepting places on Electronic Engineering degree courses.

To secure a sustainable supply of quality and industry-prepared graduates

UKESF is helping to attract, prepare and retain talent for the UK electronics industry to maintain and grow its global leadership position.

How does UKESF work?

UKESF offers a sector-specific programme for employers to engage with young people at school and university through to graduate employment, by sponsoring and participating in a programme that is:

Raising awareness in schools of the value of electronics to society and the economy

Through a network of "Champions for Engagement", UKESF is supporting ***Employer Engagement with Schools*** via established national programmes that promote science, technology, engineering and maths (STEM).

Attracting school students to degrees and careers in Electronic Engineering

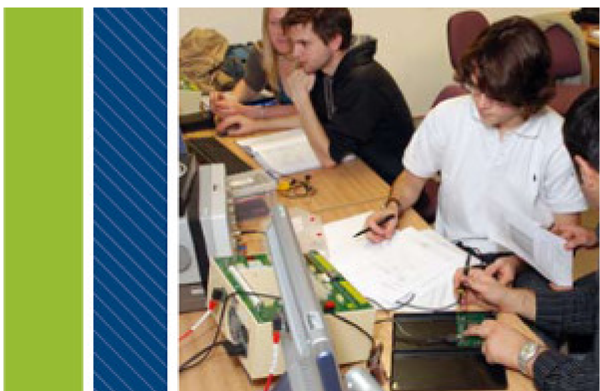
UKESF is working in partnership with Headstart[1] to deliver residential ***Summer Schools*** for talented 17 year-olds to experience a taste of degree study in Electronic Engineering and to learn about advances and careers in the sector.

Facilitating relationships between companies and university students

Through its ***Scholarship Scheme,*** UKESF matches high-calibre undergraduate students at leading UK universities with companies for sponsorship and practical experience of the industry through mentoring and work placements.

Securing employment for graduates

Through its ***Graduate Placement Scheme***, UKESF will help place graduating scholars with employers through its network of companies where sponsors are unable to offer employment.



Who is involved?

Founder Partners establishing UKESF and providing strategic direction

- UKESF has been established with funding from NMI[2], BIS[3], Semta[4] and its industry founders.
- The programme is being delivered in collaboration with leading UK universities.

Industry sponsors

Industry support and sponsorship are key to the success of UKESF. NMI, Semta and the UK Electronics Alliance are working together to engage employers with the programme.

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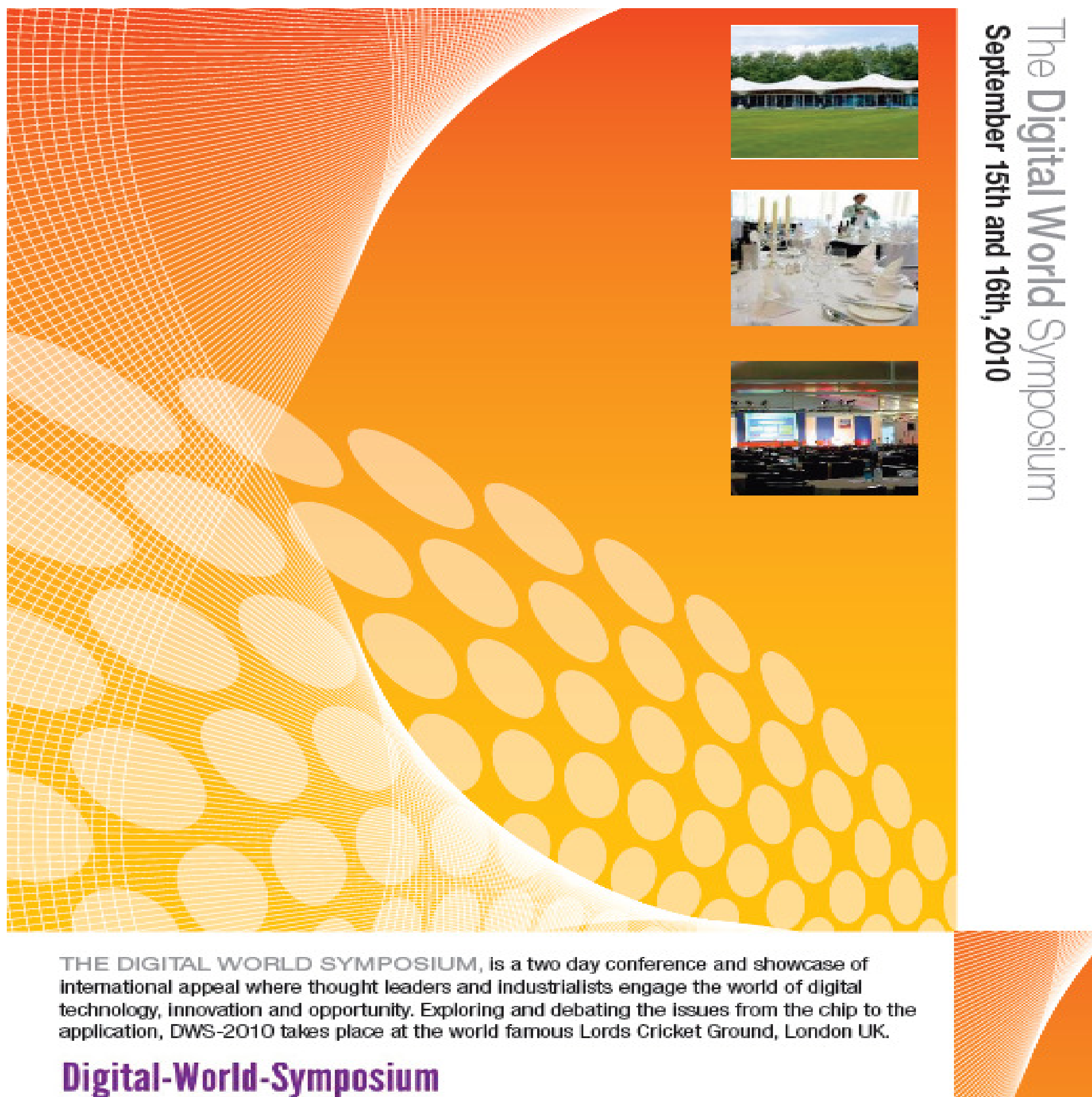
[1] Headstart is an Engineering Development Trust programme
[2] National Microelectronics Institute
[3] Department for Business Innovation and Skills
[4] Sector Skills Council for Science, Engineering and Manufacturing Technologies

7 Digital World Symposium

Announcing The Digital World Symposium - a summit event requested by NMI members, associate technology producers and users. Taking place on **Sept 15th and 16th** at **Lords Cricket Ground** London, DWS 2010 brings together high value parts of the electronics supply chain from technology providers, business and commercial users, to market and standards influencers. This is a flagship event hosted by NMI in the UK and provides the opportunity to learn about key market sector developments for smart, connected and electronically enabled technologies plus the opportunity to showcase and make new partner engagements. ***Not to be missed!***

Register online now at: http://bit.ly/DWS2010-Register



8 NMI Network Events, Conferences, Forums & Annual Awards Dinner – 2010 Programme

Date	Event
16th Feb	Operations Forum, Swindon
24th Feb	Quality & Reliability Excellence Network, Teddington *"Cutting Corners Costs Quality"*
25th Feb	Supplier Forum, Towcester
29th Apr	Analogue/Mixed-Signal/RF Innovation Network, Swindon "Internet Everywhere - Energy & Bandwidth Challenges"
25th May	**System-Level Design/Packaging Innovation Network, Cambridge** ***"Lifting the Lid on Product Design"***
22~23rd Jun	**Low-Carbon Innovation Network, University of Warwick** ***"Automotive Electronics"***
29th Jun	**Verification Excellence Network, Didcot** ***"Verification Roadmapping Projects"***
9th Sep	**NMI/GSA Supplier Forum, London** ***"Chip Security"***
15th-16th Sep	**Digital World Symposium, London**
6th Oct	**Embedded Software & Systems Innovation Network**
20th Oct	**Operations Forum, Cambridge**
4th Nov	**NMI Annual Awards Dinner, London**
23rd Nov	**Design for Manufacture Excellence Network** **"Managing Test Cost & Complexity"**

See Events Calendar on www.nmi.org.uk for latest updates, full details, contacts and registration.
* = dates and locations are subject to confirmation.

Speakers and Sponsors Wanted

If you are interested in participating in NMI Networks or would like to raise your company profile through sponsoring a network, event or tabletop please contact robin.kennedy@nmi.org.uk for initial enquiries.

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9 Additional Information

SYNOPSYS®

Synopsys, Inc.

Rapid Prototyping Made Easy With The Confirma Rapid Prototyping Platform

Overview

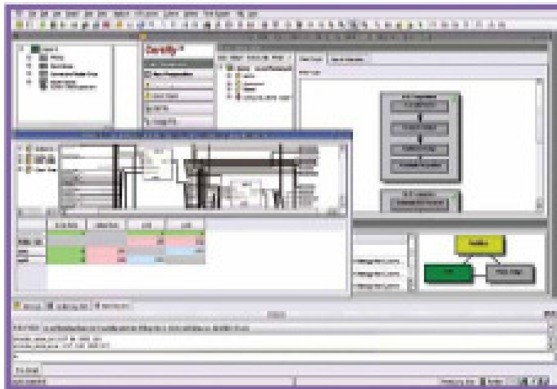
ASIC designs continue to increase in size, complexity, and cost. At the same time, aggressive competition makes today's electronics markets extremely sensitive to time-to-market pressures. Furthermore, market windows are continually narrowing.. Failing to have a product available at the beginning of the intended market window may result in significantly reduced revenue.

These factors have dramatically increased the pressure for ASIC designs to be "right-first-time" with no re-spins. In turn, this has driven the demand for fast, efficient, and cost-effective verification at both the chip and system levels.

The Confirma™ Rapid Prototyping Platform from Synopsys provides a tightly-integrated, easy to-use, and comprehensive at-speed verification environment that dramatically accelerates the functional verification of ASICs and ASSPs.

Three Major Components of the Confirma Platform

The Certify® Multi-FPGA implementation and partitioning software

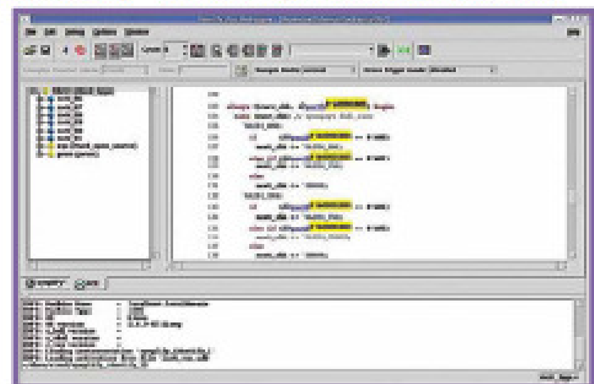


The Certify tool provides a quick and easy way to partition large ASIC designs into multi-FPGA prototyping boards. Certify includes features that make it easy to adapt to your existing device flow to get you up and running quickly.

Key Features of the Certify software:

- Easy to use graphical user interface flow guide
- Automatic and manual partitioning
- Uses Synopsys Design Constraints to manage timing
- Tightly integrated with Confirma flow hardware
- Supports multi-core parallel processing for faster runtimes
- Supports most leading FPGA devices
- Industry-leading Synplify Premier synthesis engine

The Identify® Pro visibility enhancement software



The Identify Pro software, featuring the patented TotalRecall™ technology provides full visibility into complex FPGA-based ASIC/ASSP/SoC prototypes enabling designers to find bugs at hardware speed and debug the cause of the error in a familiar simulation environment. Identify Pro software works in a complementary manner with other verification methodologies, such as assertion-based verification and simulation, significantly improving overall productivity.

The CHIPit™ and HAPS™ Rapid Prototyping Systems

The CHIPit family of hardware and software tools features a programmable interconnect architecture for greater automation and provides emulation-like capabilities optimized for transaction-based verification. The affordable HAPS family of rapid prototyping boards is ideal for wide deployment so as to facilitate early embedded software development.

The Confirma platform is ideal for ASIC/ASSP/SoC design and verification teams who leverage FPGA-based prototypes to improve their time-to-market, to start embedded software development early and to avoid costly device re-spins. The Confirma platform achieves this by facilitating front-end architectural exploration and front-end verification by:

- Helping the hardware design engineers to quickly track down the last few hard-to-find hardware bugs
- Allowing the software development engineers to start earlier in the design cycle
- Integrating hardware and software well ahead of chip fabrication

10 About NMI

"Strengthening the Business of Microelectronics & Driving the Processes of Innovation"

The National Microelectronics Institute (NMI) is the trade association representing the semiconductor industry in the UK and Ireland.

Its aim is to help build and support a strong semiconductor community by acting as a catalyst and facilitator for commercial and technological development.

A not-for-profit organisation funded by its members, the NMI has a membership that spans the supply chain and includes fabless semiconductor manufacturers, IDMs, foundries, design services, IP providers, research/ academic institutions and business associates.

The NMI's work includes:

- Encouraging innovation, communication and collaboration through networking, brokering and sign-posting activities.
- Representing the microelectronics sector to government, policy makers and regulators.
- Supporting skills development, education and training.
- Helping to improve operational efficiency through benchmarking and best practice initiatives.
- Providing an industry specific information flow.

More information can be found at: **www.nmi.org.uk**

General Enquires:

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