



International Conference on CMOS Variability:

“The Impact of Variability on Design”

Book the Date! Tue 23rd Oct 2007

At the Royal College of Physicians, London NW1 4LE

Conference Overview: “It’s the end of the line!”

Fundamental changes are in sight that will have a far-reaching impact for design and production in the semiconductor industry - the days of happy scaling are at an end. Variability has been recognised as an emerging issue in the large semiconductor companies for a decade or more however the time is fast approaching when the repercussions will be felt throughout the industry: manufacturing technology may no longer shield design from parametric and reliability concerns. 65nm has been relatively easy, with nodes at or below 45nm significant changes take place which challenge yield, reliability and the power consumption of digital circuits. For example, SRAM has been identified as one of the first casualties and this will have a resultant impact on System-on-Chip products.

The industry must learn *“how to cope”* with variability issues across three major areas: chip design, design automation tools and manufacturing technology. Designers will need to learn how to design reliable systems on unreliable technology. Tool providers will need to change from a deterministic paradigm to statistical approaches that go beyond 3D simulations which in turn places demands on computational resources. As design margins continue to decrease, foundries will need to change from providing design rules to supplying design models.

Conference Theme

“Coping” mandates integrated-working between designers, tool providers and manufacturing partners to address the issues effectively and efficiently. How prepared is your organisation to understand the implications of these changes and manage the impact? This event provides a unique opportunity for CTO’s, engineering managers, system and chip designers, product engineers, technology developers, EDA suppliers and wafer foundries to gain crucial insight from recognised world experts.

Delegates can expect a full treatment of the subject from the leading world experts - *“fast paced with high impact”* - do not expect an easy day out! Networking with your peers and the experts cannot be understated - can you afford to miss it?

Satellite Events for Delegates:

In addition to the main conference, delegates are offered the opportunity to attend two complementary reviews of major research projects organised by Professor Asen Asenov. Interested parties should indicate their interest when registering for the main conference as satellite event registration is not automatic.

22 October: *“Meeting the material challenges of nano-CMOS electronics”*

24 October: *“Meeting the design challenges of nano-CMOS electronics”*

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Conference Agenda

8:30 Registration and Refreshments

9:00 Welcome & Introduction



Rt. Hon. Stephen Timms MP, Minister for Competitiveness
"Welcome to the CMOS Variability Conference"



Key Note by Asen Asenov, University of Glasgow
"Variability in the next generation CMOS technologies and impact on design"

9:40 SESSION 1: Design Concepts

Bart Dierickx, IMEC: "Technology aware design"

Steve Furber, University of Manchester: "Dealing with variability in modern circuit design"

Masami Murakata, STARC: "DFM&Y- Research and development topics in STARC"

*** Coffee ***

11:30 SESSION 2: Design Implementation & Tools

Christophe Guittard, Mentor Graphics: "The serious impact of "variability" on traditional Place & Route"

Victor Moroz, Synopsys: "OPC corrections and strain - the impact on design"

Pierrick Pedron, Cadence: "SOC Encounter Statistical Design"

*** Buffet Lunch & Networking ***

14:00 SESSION 3: Semiconductor Technologies

David Frank, IBM: "High Performance CMOS variability in the 65nm regime and beyond"

Marcel Pelgrom, NXP Semiconductors: "Nanometer CMOS is a statistical challenge!"

Walter Ganzevles, TSMC: "Solutions for managing increased variability"

*** Coffee ***

15:50 SESSION 4: IP Development & Research

Yves Laplanche, ARM: "IP design: how sigma is changing our lives?"

16:15 PANEL: "Integration and Collaboration in the Era of Design for Variability (DFV)"

Chair: Asen Asenov

17:00 Conference Close immediately followed by:

Post-Conference Drinks Reception & Further Networking



Conference Registration:

Register from the NMI website http://www.nmi.org.uk/events/DFM_23102007.htm

Or by sending an email to dfm@nmi.org.uk

Delegate rates:

£295 – Standard Delegate Rate

£195 – NMI members & Promotional Partners

£195 – Academia and Research Institutes

(Note: Prices shown do not include Value Added Tax at 17.5%)

Delegate rate includes attendance of the full conference on 23rd Oct, refreshments, lunch, post-conference drinks reception, printed conference proceedings and access to the workshops being held on 22nd and 24th October. Delegates can check whether their organisation is an NMI member from the website:

http://www.nmi.org.uk/about/current_members.htm

We will confirm your on-line registration and payment with an email and you will receive an electronic ticket. Your payment must be made prior to the event date. Registration is not complete until you have received confirmation.

Cancellations

All cancellations must be made by email to NMI at dfm@nmi.org.uk by 9th October 2007. Such cancellations will receive a refund subject to a handling and administration charge of £35 + VAT per ticket. Cancellations post 9th October 2007 will not be eligible for a refund. NMI reserves the right to make changes to the programme, location and/or speakers without prior notice. NMI will not offer refunds to delegates due to terrorist alert or incident unless the conference is cancelled. In this instance, NMI will retain up to 50% of the conference fee to cover marketing, administration and delegate registration costs.

Conference Venue:

The Royal College of Physicians is a prestigious venue in a convenient and attractive location in central London, easily accessible by all forms of transport. The main entrance and reception face Regent's Park, on the park's 'Outer Circle':

The nearest underground stops are:

- Regent's Park station on the Bakerloo line (3 minutes walk)
- Great Portland Street Station on the Circle, Metropolitan and City lines (5 minutes walk)

For further travel details see <http://www.rcplondon.ac.uk/venue/location.htm>



Accommodation for Conference Delegates:

Delegates benefit from preferential rates at the following nearby hotels

- **Langham Hotel** <http://london.langhamhotels.com/>
- **Thistle Euston**
http://www.thistlehotels.com/thistle/hotels/hotelFinder/viewHotel.do?_DARGS=/thistle/WEB-INF/portlets/thistleLocationInfo/index.jsp.7_A&_DAV=th-euston
- **Melia White House** <http://www.melia-whitehouse.com/en/melia-white-house.html>

In case of difficulty reserving accommodation, contact us at dfm@nmi.org.uk

Delegate Access & Additional Requirements

Vegetarians are catered for with the buffet lunch however if you have any other dietary or access requirements please notify us at the time of registration.

About the Satellite Events

The satellite events will consist of half-day reviews, where delegates will be introduced to the research highlights from two major multidisciplinary UK EPSRC projects in the field of device, circuit and systems design.

22 October: "Meeting the material challenges of nano-CMOS electronics" - Investigates the impact of the atomic and electronic structure of materials on nano-scale electronics. Project partners UCL, Glasgow University and NASA ARC will present research aimed at developing tools capable of simulating the properties of materials, device interfaces and interface defects. This involves the application of atomic and electronic structure calculations, Non-equilibrium Green's Function transport calculations and 3D atomistic device simulations.

24 October: "Meeting the design challenges of nano-CMOS electronics" – A UK eScience pilot project investigating the impact of parameter fluctuations on next generation circuits and the design methodologies that will be required to make them. Project partners in the Universities of Glasgow, Manchester, Southampton, Edinburgh and York will present initial research into the development of new TCAD and ECAD 'grid' enabled simulation methodologies capable of tackling the design complexity of nano-CMOS electronics that specifically result from device variability.

Sponsored by:



EPSRC is the main UK government agency for funding research and training in engineering and the physical sciences, investing around £740 million a year in a broad range of subjects – from mathematics to materials science, and from information technology to structural engineering. They operate to meet the needs of industry and society by working in partnership with universities to invest in people and scientific discovery and innovation.

About NMI

NMI is a not-for-profit organisation funded by its members and includes fabless semiconductor companies, intellectual property providers, contract design services, integrated device manufacturers, semiconductor manufacturers, vendors, service providers, research and academic institutions.

Key work streams include:

- Encouraging innovation, communication and business collaboration through sector networks.
- Representation to government, policy makers and regulators.
- Skills development, education and training.
- Supply chain efficiencies through benchmarking and best practice.
- Information provision.

See www.nmi.org.uk and click on events for full schedule of NMI Network Events

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